JP 7-84879 Machine Translation

[Claim(s)]

[Claim 1] In the cache memory equipment of the write back method equipped with the cache for storing some copies of the contents of the main memory by a line unit [in response to the memory access demand from the use equipment of said main memory, judge the hit/miss hit of whether the data of the request destination exists in said cache, and also] The write-back cache control means which performs control for carrying out write back of the updated data on the cache which has not been returned to said main memory to said main memory per cache line, The lead sequencer which reads the data for one cache line from said main memory to a cache, The Rheydt sequencer which performs write operation demanded by said use equipment on the cache line of said cache, It is the Rheydt mistake sequencer started according to the Rheydt mistake detection by said write back control means. In the state of the continuation write operation which starts the account Rheydt sequencer of back to front which started said lead sequencer in the normal state, and writes and changes all one cache lines on said cache Cache memory equipment characterized by providing the Rheydt mistake sequencer which starts said Rheydt sequencer without starting said lead sequencer.

[Claim 2] Cache memory equipment according to claim 1 characterized by providing further a judgment means to judge whether it is in the continuation write operation state which writes and changes all one cache lines on said cache, and to notify the judged result to said Rheydt mistake sequencer.

[Claim 3] Provide further the judgment conditioning means for setting up the memory

area which is the target of said continuation write operation as judgment conditions used for the above-mentioned judgment by said judgment means, and [said judgment means] Cache memory equipment according to claim 2 characterized by performing the above-mentioned judgment based on the judgment conditions and demand access point which are set as said judgment conditioning means when the memory access of the Rheydt specification is required from said use equipment.

[Claim 4] Cache memory equipment according to claim 3 characterized by performing a setup of said judgment conditions to said judgment conditioning means by software processing.

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the cache memory equipment of a write back method suitable at the time of the Rheydt mistake generating with the cache in which some copies of a main memory are placed.

[0002]

[Description of the Prior Art] When the Rheydt mistake occurred to the write request from CPU conventionally with the cache memory equipment of the write back method equipped with the cache with which some copies of a main memory are placed, it was common that the following cache control was performed by the Rheydt mistake sequencer.

[0003] First, the corresponding data portion on the main memory for cache 1 linesize

which a lead sequencer is started by the Rheydt mistake sequencer and contains the data of the write request point is once read into a cache line.

[0004] Next, the Rheydt sequencer is started by the Rheydt mistake sequencer and a change (updating) of the data of the part corresponding to the write request point is made on the cache line.

[0005] The cache line after this data changing is the target of write back, and write back is carried out to a main memory using the idle time of CPU etc. (returned). As a result, parts for all the applicable data division on a main memory are replaced with the data of the cache line concerned. The data updating result performed on the cache line according to the write request from CPU is reflected in the corresponding section of those for the data division on the main memory corresponding to the one line (write request point from CPU). On the other hand, the contents after the write back of other parts are maintained by the right state in accordance with the original contents.

[0006]

[Problem to be solved by the invention] Once it read a part for the applicable data division on the main memory for cache 1 linesize into the cache line when the Rheydt mistake occurred in a cache conventionally as described above, it was common to have changed the demanded data on the cache line.

[0007] Thus, the data which read a part for a main memory data division for cache 1 linesize into the cache line, and was demanded is changed in order that the contents of the part which had not been the target of change may not be changed by the write back to a main memory.

[0008] However, in this conventional system, since reading for the cache of one line into

a cache from a main memory occurred at every generating of the Rheydt mistake, when the generating frequency of the Rheydt mistake increased, the transaction of Bath also increased, and there was a problem that performance fell.

[0009] This invention was made in consideration of the above-mentioned situation, and [that purpose] It may turn out beforehand that the whole of one line on a cache is rewritten, and [in such a case] Even if it does not read the data for one line from a main memory according to the Rheydt mistake generating It notes not producing un-arranging according to the write back to a main memory at all. It is in offering the cache memory equipment which can aim at reduction of the transaction of Bath by controlling reading of the corresponding data portion from the main memory at the time of the Rheydt mistake generating when it turns out beforehand that the whole of one line on a cache is rewritten.

[0010]

[Means for solving problem] This invention receives the memory access demand from the use equipment of a main memory in the cache memory equipment of a write back method. [judge the hit/miss hit of whether the data of the request destination exists in a cache, and also] The write-back cache control means which performs control for carrying out write back of the updated data on the cache which has not been returned to a main memory to a main memory per cache line, The lead sequencer which reads the data for one cache line from a main memory to a cache, The Rheydt sequencer which performs write operation demanded by main memory use equipment on the cache line of a cache, It is the Rheydt mistake sequencer started according to the Rheydt mistake detection by a write back control means. In the state of the continuation write operation which starts the Rheydt sequencer after starting a lead sequencer in a normal state, and

writes and changes all one cache lines on a cache It is characterized by having the Rheydt mistake sequencer which starts the Rheydt sequencer without starting a lead sequencer.

[0011] Moreover, this invention judges whether it is in the continuation write operation state which writes and changes all one cache lines on a cache, and is characterized also by having further a judgment means to notify that judged result to the Rheydt mistake sequencer.

[0012] Moreover, this invention is further equipped with the judgment conditioning means for setting up the memory area which is the target of continuation write operation as judgment conditions which the above-mentioned judgment means uses. It is characterized also by performing the above-mentioned judgment by a judgment means based on this judgment condition and a demand access point from main memory use equipment at a memory right access demand.

[0013]

[Function] [with the main memory right access which the main memory (CPU etc.) use equipment generated from now on follows in the above-mentioned composition] When it turns out beforehand that the whole of one line on a cache is rewritten, the judgment conditions which consist of size which shows the start address and range of the right access by specification of software, for example are set as a judgment conditioning means.

[0014] A judgment means notifies condition formation to the Rheydt mistake sequencer, when the demanded Rheydt address judges whether it enters in the address range which the judgment conditions set as the judgment conditioning means show and is contained, if there is a main memory right access demand from main memory use equipment.

[0015] On the other hand if a write-back cache control means has the main memory right access demand from main memory use equipment The existence of the hit/miss hit at whether the data of the demanded right access point exists in a cache and the time of Rheydt is investigated, and the result is notified to the Rheydt mistake sequencer.

[0016] The Rheydt mistake sequencer will investigate whether condition formation (shown judged result) is notified from the judgment means, if the Rheydt mistake is notified from a write-back cache control means. If condition formation is notified, [the Rheydt mistake sequencer] The Rheydt sequencer is started without not starting a lead sequencer's by a judgment means judging it as what is directed, not starting the Rheydt sequencer, after starting a lead sequencer like before, but starting a lead sequencer.

[0017] Thus, when the main memory right access demand from main memory use equipment has agreed on the conditions which a judgment conditioning means shows, That is, when it is main memory Rheydt where the whole of one line on a cache is rewritten, since data reading into a cache from the main memory by a lead sequencer is not performed, reduction of the transaction of Bath can be aimed at.

[0018] And even if data reading into a cache from a main memory is not performed Since the whole of one line on a cache is rewritten by continuous right access, even if write back of the data of the cache line concerned is carried out to a main memory by write back control of a write-back cache control means from a cache after that, it is satisfactory in any way.

[0019]

[Working example] Drawing 1 is the block diagram showing the composition of the cache memory equipment of the write back method concerning one work example of this

invention. In this figure, it is the external bus to which the cache memory equipment of a write back method connects 1 to, a main memory is connected to 2, and cache memory equipment 1 and the main memory 2 are connected 3.

[0020] Cache memory equipment 1 has a cache 11, the write-back cache control section 12, the judgment conditioning section 13, the judgment section 14, the lead sequencer 15, the Rheydt sequencer 16, and the Rheydt mistake sequencer 17.

[0021] A cache 11 is used for storing some copies of the contents of the main memory 2 per line (block). However, in this example, since the write back method is applied, the contents of the cache line of a cache 11 are not always the same as that of the corresponding data portion of the main memory 2. In this main memory 2, the cache line from which the contents differ is called a dirty cache line, and it is the target of the write back (write return) to the main memory 2.

[0022] The write-back cache control section 12 is what manages control of the cache memory equipment 1 whole. [in response to the memory access demand from CPU (not shown), judge the hit/miss hit of whether the data of the request destination exists in a cache 11, and also] Control for returning the control for carrying out write back of the updated data on the cache 11 which has not been returned to the main memory 2 to the main memory 2 per cache line, i.e., the data of a dirty character, to the main memory 2 etc. is performed. The tag memory for this cache control (directory memory) is omitted.

[0023] [the judgment conditioning section 13] when the Rheydt mistake is detected by the write-back cache control section 12 It is for setting up the conditions (judgment conditions) used for the judgment of whether it is necessary to read into a cache 11 the corresponding data portion on the main memory 2 for cache 1 linesize containing the data

of the write request point. Main memory right access from CPU is performed continuously, this judgment condition is set up by specification of software, when it turns out beforehand that the whole of one line on a cache 11 is rewritten, and it consists of size which shows the start address and range of that right access. Then, the judgment conditioning section 13 consists of an address register 131 with which the above-mentioned start address is set up for a setup of this judgment condition, and a size register 132 with which size is set up.

[0024] The judgment section 14 judges whether the main memory right access demand from CPU agrees on the judgment conditions set as the judgment conditioning section 13. The lead sequencer 15 reads the data for one cache line from the main memory 2 to a cache 11.

[0025] The Rheydt sequencer 16 performs the writing to a cache 11. The Rheydt mistake sequencer 17 controls operation at the time of the Rheydt mistake judging by the write-back cache control section 12, and determines whether start the lead sequencer 15 based on the judged result of the judgment section 14.

[0026] Next, operation of the composition of drawing 1 is explained with reference to the flow chart of drawing 2 . First, it is assumed that the main memory right access which CPU to be generated from now on follows shows beforehand that the whole of one line on a cache 11 is rewritten.

[0027] [with in such a case, specification (operation of CPU which follows) of software] The information which consists of the start address and size of the range of the continuation access is set as the judgment conditioning section 13 as judgment conditions whether it is necessary to read the data for cache 1 linesize into a cache 11 from the main

memory 2 at the time of the Rheydt mistake. The start address in a judgment condition is set as the address register 131 in the judgment conditioning section 13, and, specifically, the size in the judgment condition concerned is set as the size register 132 in the judgment conditioning section 13, respectively.

[0028] It is cases, such as a 1-page zero clear in the memory management of an operating system (OS), the case of a block copy, etc. that such judgment conditioning is performed, for example.

[0029] Now, the address and control signal for main memory right access should be outputted from CPU after the above judgment conditioning operation. This address and control signal are led to the write-back cache control section 12 and the judgment section 14.

[0030] When, as for the write-back cache control section 12, the control signal from CPU shows the write request, The existence of the hit/miss hit at whether the data of the right access point which the address from this CPU specifies is stored in the cache 11, and the time of Rheydt is investigated, and the result is notified to the Rheydt mistake sequencer 17. Operation of the write-back cache control section 12 here is the same as usual.

[0031] When, as for the judgment section 14, the control signal from CPU shows the write request on the other hand, The address from this CPU judges whether it enters in the address range shown on the judgment conditions set as the judgment conditioning section 13, i.e., the address range for the size which the size register 132 which begins from the address which an address register 131 shows shows.

[0032] The judgment section 14 is restricted when the address from CPU is contained in the above-mentioned address range. That is, the control signal from CPU shows a write

request, and when the address from CPU has agreed on the judgment conditions which the judgment conditioning section 13 shows, it restricts, and condition formation is notified to the Rheydt mistake sequencer 17.

[0033] If the Rheydt mistake is notified from the write-back cache control section 12, the Rheydt mistake sequencer 17 will perform processing according to the flow chart of drawing 2 so that it may state below.

[0034] The Rheydt mistake sequencer 17 investigates first whether condition formation (shown judged result) is notified from the judgment section 14 (Step S1). If condition formation is notified, the Rheydt mistake sequencer 17 will judge it as that it is instructed to be not to start the lead sequencer 15 by the judgment section 14. In this case, the Rheydt mistake sequencer 17 starts the Rheydt sequencer 16 immediately, without not starting the Rheydt sequencer 16, after starting the lead sequencer 15 like before, but starting the lead sequencer 15 (Step S2).

[0035] Namely, the Rheydt mistake sequencer 17 starts the Rheydt sequencer 16, without reading the corresponding data portion on the main memory 2 for cache 1 linesize containing the data of the write request point. The data of the position corresponding to the write request point on 1 cache line of a cache 11 is made to be rewritten from CPU to the Rheydt data.

[0036] In this case, since data reading into a cache 11 from the main memory 2 by the lead sequencer 15 is not performed, the transaction of the external bus 3 decreases.

[0037] Here, the cache line on the cache 11 which is the target of rewriting (shown line address) is determined by the write-back cache control section 12. When the contents of this determined cache line have been the targets of the write back to the main memory 2,

after the write-back cache control section 12 returns the data of this line to the main memory 2, the above-mentioned rewriting is performed.

[0038] on the other hand, when condition failure is notified from the judgment section 14 The Rheydt mistake sequencer 17 starts the lead sequencer 15 first like before (Step S3). After making the corresponding data portion on the main memory 2 for cache 1 linesize containing the data of the write request point read into a cache 11, the Rheydt sequencer 16 is started (Step S4).

[0039] In addition, when the Rheydt hit is detected by the write-back cache control section 12, the Rheydt sequencer 16 is started and the data of the position corresponding to the write request point on the cache line of the hit cache 11 is rewritten from CPU to the Rheydt data.

[0040] [as mentioned above, the request destination of the main memory right access which continues from CPU according to this example] As long as it enters in the address range which the judgment conditions set as the judgment conditioning section 13 show Even if the Rheydt mistake occurs, the lead sequencer 15 is not started, but for this reason, reading for one line which is applicable into a cache 11 from the main memory 2 is not performed, but data rewriting on the cache line of a cache 11 is only performed by the Rheydt sequencer 16.

[0041] The cache line concerned of this cache 11 will be altogether rewritten from CPU to the Rheydt data, if the above-mentioned main memory right access is performed continuously. [with therefore, write back control of the after that and write-back cache control section 12] When write back of the data of the cache line concerned is carried out to the main memory 2 from a cache 11, it means rewriting correctly parts for all the

applicable data division on the main memory 2 from CPU to the Rheydt data.

[0042] namely, when the request destination of the main memory right access which continues from CPU is contained in the address range which the judgment conditions set as the judgment conditioning section 13 show Even if it performs data rewriting on a cache 11 without starting the lead sequencer 15 at the time of the Rheydt mistake generating (based on the Rheydt sequencer 16), parts for all the applicable data division on the main memory 2 are rewritten by right data by the write back after continuation access.

[0043] In addition, in said work example, main memory right access from CPU is performed continuously. When it turned out beforehand that the whole of one line on a cache 11 is rewritten, the case where the size which shows the start address and range of the right access was used as judgment conditions was explained, but it does not restrict to this.

[0044] For example, if it is in the system which applies a paging system [each entry of the page table showing the correspondence relation between a page and the memory area on a main memory (2)] The flag bit which shows whether access to a correspondence page is performed continuously is prepared, and you may make it turn on the flag hit of the corresponding entry in a page table in the case of the zero clear of the page concerned in the memory management of OS etc. What is necessary is just to notify condition formation from the judgment section 14 to the Rheydt mistake sequencer 17 during the period of the main memory right access for the page concerned by this method.

[0045]

[Effect of the Invention] As explained in full detail above, according to this invention, it

can set in the continuation write operation state where the whole of one line on a cache is rewritten. As opposed to the demand which judges the main memory right access demand from main memory use equipment, and agrees on this condition By operating the Rheydt sequencer immediately, without operating a lead sequencer, even if it is at the Rheydt mistake detection time Since it had composition to which the writing on the cache line concerned is made to carry out, without reading the corresponding data portion from a main memory to a cache line, the transaction of Bath can be decreased and improvement in performance can be aimed at. And even if data reading into a cache from a main memory is not performed Since the whole of one line on a cache is rewritten by continuous right access, even if write back of the data of the cache line concerned is carried out to a main memory by write back control of a write-back cache control means from a cache after that, it is satisfactory in any way.